LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A digital radio frequency (RF) transceiver circuit, comprising:

a converter circuit that samples a receiver input signal;

circuitry that is adapted to select between a transmitter input signal and the sampled receiver input signal, the transmitter input signal including a real portion and an imaginary portion;

a filter, the filter being adapted to receive both the transmitter input signal and the sampled receiver input signal, the filter adapted to produce either a filtered transmitter signal or a filtered receiver signal, the filter further including at least two filter elements operating in parallel; and

circuitry that alternatively receives the filtered transmitter signal or the filtered receiver signal and produces a modulated output and a demodulated output, the demodulated output including a real portion and an imaginary portion,

wherein the filter operates at a sampling frequency that is lower than the sampling frequency of the converter and the circuitry that produces the modulated output.

2. (previously presented) The RF transceiver circuit set forth in claim 1. wherein the filter comprises four filters that employ impulse response characteristics set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

3. (previously presented) The RF transceiver circuit set forth in claim 1, wherein the filter comprise finite impulse response (FIR) filters.

4. (previously presented) The RF transceiver circuit set forth in claim 3, wherein the filter comprises four filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

5. (previously presented) The RF transceiver circuit set forth in claim 1, wherein the RF transceiver circuit comprises a portion of an orthogonal frequency division multiplexing (OFDM) transceiver.

6. (previously presented) The RF transceiver circuit set forth in claim 1, wherein outputs from at least a portion of the plurality of filters are delivered as inputs to a multiplexer that provides the modulated output.

7. (previously presented) The RF transceiver circuit set forth in claim 1, wherein the modulated output is processed by a digital-to-analog (D/A) converter at a frequency four times greater than a frequency of a carrier of the modulated output.

8. (previously presented) The RF transceiver circuit set forth in claim 1, wherein the receiver input signal is processed with a delay line having a plurality of output delays, each of the output delays corresponding to one of the plurality of filters and wherein each of the plurality of filters has a different delay characteristic that compensates the associated output delay.

9. (currently amended) A digital radio frequency (RF) transceiver circuit, comprising:

means for sampling a receiver input signal;

means for selecting between a transmitter input signal and the sampled receiver input signal, the transmitter input signal including a real portion and an imaginary portion;

means for receiving either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal; and

means for alternatively receiving the transmitter signal or the receiver signal and for producing a modulated output and a demodulated output, the demodulated output including a real portion and an imaginary portion, wherein the means for receiving includes means for processing both the transmitter input signal and the receiver input signal in a filter at a sampling frequency that is lower than the sampling frequency in the means for sampling, the filter further including at least two filter elements operating in parallel.

10. (previously presented) The RF transceiver circuit set forth in claim 9. wherein the means for receiving either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal comprises four filters that employ impulse response characteristics set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

11. (previously presented) The RF transceiver circuit set forth in claim 9, wherein the means for receiving either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal plurality of filters comprise a plurality of finite impulse response (FIR) filters.

12. (previously presented) The RF transceiver circuit set forth in claim 11, wherein the plurality of FIR filters comprises four FIR filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

13. (previously presented) The RF transceiver circuit set forth in claim 9, wherein the RF transceiver circuit comprises a portion of an orthogonal frequency division multiplexing (OFDM) transceiver.

14. (previously presented) The RF transceiver circuit set forth in claim 9, wherein the means for alternatively receiving the transmitter signal or the receiver signal and for producing a modulated output and a demodulated output comprises a multiplexer that provides the modulated output.

15. (previously presented) The RF transceiver circuit set forth in claim 9, wherein the modulated output is processed by a digital-to-analog (D/A) converter at a frequency four times greater than a frequency of a carrier of the modulated output.

16. (previously presented) The RF transceiver circuit set forth in claim 9, wherein the means for receiving either the transmitter input signal or the receiver input signal and for producing either a transmitter signal or a receiver signal comprises a plurality of filters and wherein the receiver input signal is processed with a delay line having a plurality of output delays, each of the output delays corresponding to one of the plurality of filters and wherein each of the plurality of filters has a different delay characteristic that compensates the associated output delay.

17. (currently amended) A method of processing signals in a digital radio frequency (RF) transceiver circuit, the method comprising:

sampling a receiver input signal;

selecting between a transmitter input signal and the sampled receiver input signal, the transmitter input signal including a real portion and an imaginary portion;

receiving either the transmitter input signal or the receiver input signal and producing either a filtered transmitter signal or a filtered receiver signal; and

alternatively receiving the filtered transmitter signal or the filtered receiver signal and producing a modulated output and a demodulated output, the demodulated output including a real portion and an imaginary portion, wherein the step of receiving includes processing both the transmitter input signal and the receiver input signal in a filter at a sampling frequency that is lower than the sampling frequency in the sampling step, the filter further including at least two filter elements operating in parallel.

18. (previously presented) The method set forth in claim 17, comprising alternatively processing the transmitter input signal or the receiver input signal with at least four filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

19. (previously presented) The method set forth in claim 17, comprising creating the transmitter input signal and the receiver input signal using an orthogonal frequency division multiplexing (OFDM) strategy.

20. (previously presented) The method set forth in claim 17, comprising processing the modulated output using a digital-to-analog (D/A) converter at a frequency four times greater than a frequency of a carrier of the modulated output.

21. (previously presented) A digital radio frequency (RF) transceiver circuit, comprising:

circuitry that is adapted to select between a transmitter input signal and a receiver input signal;

a plurality of filters that are adapted to receive either the transmitter input signal or the receiver input signal and to produce either a filtered transmitter signal or a filtered receiver signal; and

circuitry that alternatively receives the filtered transmitter signal or the filtered receiver signal and produces a modulated output and a demodulated output,

wherein the plurality of filters employ impulse response characteristics set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1

22. (previously presented) A method of processing signals in a digital radio frequency (RF) transceiver circuit, the method comprising:

selecting between a transmitter input signal and a receiver input signal;

receiving either the transmitter input signal or the receiver input signal and producing either a filtered transmitter signal or a filtered receiver signal;

alternatively receiving the filtered transmitter signal or the filtered receiver signal and producing a modulated output and a demodulated output, and

wherein the step of receiving further includes the step of processing either the transmitter input signal or the receiver input signal with at least four filters that employ tap coefficient values set forth below:

	1	z^{-1}	z^{-2}	z^{-3}	z^{-4}	z^{-5}	z^{-6}	z^{-7}	z^{-8}	z^{-9}	z^{-10}	z^{-11}
FLTR0	0	-4	7	-9	12	-12	268	-12	12	-9	7	-4
FLTR1	1	0	2	-8	19	-65	-238	50	-28	16	-10	5
FLTR2	3	-6	12	-24	47	-160	-160	47	-24	12	-6	3
FLTR3	-5	10	-16	28	-50	238	65	-19	8	-2	0	-1